Cadence announces comprehensive assertion-based verification solution

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Expanded support of PSL and SystemVerilog assertions enables more efficient verification

Cadence today announced a comprehensive assertion-based verification (ABV) solution as a part of its Incisive functional verification platform. The solution speeds verification of complex designs by creating an environment that helps users define assertions correctly, enables early detection of bugs close to the source, and monitors for completeness through assertion coverage. This functionality has been integrated into the platform's Incisive Unified Simulator.

The Cadence ABV environment brings together tools, language, IP, debug and coverage. It includes broad, native assertion support for Property Specification Language (PSL), SystemVerilog Assertions (SVA) and Open Verification Library (OVL). In addition to these Accellera standards, Cadence is also introducing an extended open-source library of assertions.

"Having a verification platform support multiple design and assertion languages is very important to us," said Ulrich Hummel, manager of CAD/CAE for Micronas in Freiburg, Germany. "As we develop new design IP and integrate that with existing designs as well as 3rd party IP, we need to be able to simulate all the standard design languages. The Incisive platform allows us to do that in a common, integrated, single debug environment that supports our complete verification flow."

The new Incisive Assertions Library included in the ABV environment incorporates 50 complex assertion statements and code for customisation. This enables users to specify powerful assertion statements quickly, resulting in faster verification time and ultimately, faster time-to-market. This library will be available in both PSL and SVA languages. A sample set of library elements is available for review at http://www.cadence.com/products/functional_ver/abv_dt.aspx.

The ABV solution naturally captures design knowledge in the user's hardware description language. The combination of assertion-driven functional coverage, enhanced unified graphical user interface and debug environment for assertion functionality within the Incisive platform all greatly improves ease-of-use for the designer.

This announcement underscores the strong commitment that Cadence has for standard languages. In addition to supporting PSL assertions with Verilog and VHDL code for over two years, the Incisive Unified Simulator now supports PSL within SystemC code, OVL, and SystemVerilog Assertions. This gives customers the flexibility to use assertions in the language of their choice.

"Our assertion solution, based on open standards, provides the most advanced verification techniques available on the market today," said Mitch Weaver, vice president and general manager, Systems and Functional Verification division, Cadence. "Our customers love the fact that the Incisive approach to assertions provides a unified environment based on an integrated platform for increased verification productivity."

The comprehensive assertion solution in the Incisive Unified Simulator and the PSL-based Incisive

Assertions Library will be available in December 2004.

About Cadence

Cadence is the largest supplier of electronic design technologies and engineering services. Cadence solutions are used to accelerate and manage the design of semiconductors, computer systems, networking and telecommunications equipment, consumer electronics, and a variety of other electronics-based products. With approximately 4,850 employees and 2003 revenues of approximately $1.1 billion, Cadence has sales offices, design centers, and research facilities around the world. The company is headquartered in San Jose, Calif., and traded on the New York Stock Exchange under the symbol CDN. More information about the company, its products and services is available at www.cadence.com.

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