

XJTAG targets production sites with XJRunner add-on to boundary scan system

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* XJRunner is packed with features to simplify production line testing including logging and support for serial numbers, file locking, date and time handling etc.

CAMBRIDGE, England, December 22, 2004 - XJTAG Limited (www.xjtag.com), a specialist design and test tool developer, has developed XJRunner, a graphical add-on to its XJTAG boundary scan Development System. XJRunner is designed for production sites that need to improve and speed up the testing of densely populated printed circuit boards - particularly those with JTAG devices such as ball grid array (BGA) and chip scale devices, flip chips and other high-density packages, which cannot be tested by traditional methods.

“The trend towards smaller, more tightly packed circuit boards with less test points and more JTAG-compliant chips is forcing manufacturers to add boundary scan capability to their test regimes,” says Dominic Plunkett, chief technology officer at XJTAG. “XJRunner has been designed to meet that requirement and to provide a low cost but highly effective alternative to bed of nails testing.”

XJRunner has a user friendly graphical interface and can be configured to provide simple pass / fail or more sophisticated test routines. XJRunner can be used to test a high proportion of the circuit including JTAG and non-JTAG devices such as BGAs, CSPs, SDRAMs, Ethernet controllers, video interfaces, flash memories, FPGAs (Field Programmable Gate Arrays), microprocessors and many other devices.

XJRunner is packed with features to simplify production line testing. To ensure traceability of boards during manufacture, XJRunner provides logging and support for serial numbers. The file locking capabilities allow information to be shared safely across multiple production lines.

To ensure that the production line administrator has all relevant data to create an XJRunner project and commence testing, XJTAG has also developed XJPack. This enables the designer or developer to automatically select or 'pack' all the relevant data for a particular board - BSDL files, netlists, XJEase files, pin mapping files etc. - for forwarding to the production facility. This is particularly useful when working with contract manufacturing partners.

“XJRunner enables the test systems developed by design engineers to be taken seamlessly forward to production testing and through into field support and repair,” added Dominic Plunkett. “XJRunner offers a cost effective way of extending the power of XJTAG - minus the development capability - throughout the product lifecycle.”

The powerful and easy-to-use XJTAG Development System, launched in 2003, provides a fully-integrated environment which can migrate seamlessly through the product life cycle from early design to field support and repair. XJTAG enables circuit designers to shorten the development cycle and prototyping process by facilitating early test development, early design validation of CAD netlists, fast generation of highly functional tests and test re-use across circuits that utilise the same devices.

XJTAG test scripts are also re-usable and portable across different boards due to the novel device-centric approach that the designers have adopted. Re-usable device tests and the abstraction of device tests from both circuit detail and complexity of JTAG (Joint Test Action Group), mean that designers can quickly develop systems to debug elements of their designs and to functionally test early prototypes.

For more information about XJRunner and the XJTAG Development System, please contact XJTAG Limited, The Irwin Centre, Scotland Road, Dry Drayton, Cambridge CB3 8AR, U.K. Telephone +44 (0) 1954 213888, facsimile +44 (0) 1954 211565 or email info@xjtag.com. Alternatively visit www.xjtag.com.

About XJTAG (www.xjtag.com)

XJTAG Limited is a specialist design and test tool developer. Its JTAG (Joint Test Action Group) development system offers a competitive solution for designers and developers of electronic circuits. Utilising XJTAG allows circuit development and prototyping process to be shortened significantly by facilitating early test development, early design validation, fast development of functional tests and test re-use across circuits that utilise the same devices. The company is based in the U.K. at The Irwin Centre, Dry Drayton, Cambridge, U.K. and has a global network of distributors which includes DiagnoSYS in North America.

About the Cambridge Technology Group (www.cambridgetechgroup.com)

Cambridge Technology Group is a holding company with three wholly owned subsidiaries - Adiabatic Logic Limited, Cambridge Technology Consultants Limited and XJTAG Limited. Adiabatic Logic (www.adiabaticlogic.com) was set up to exploit a portfolio of secured patents in the low power technology arena. Adiabatic Logic's patented Intelligent Output Driver (IOD), launched in May 2003, delivers significant (up to 75%) power savings in chip I/O for portable devices such as laptop computers, personal digital assistants (PDAs), MP3 players and smartphones.

Cambridge Technology Consultants (www.camtechconsultants.com) offers its clients - companies such as ARM, AT&T, BOC Edwards, Celoxica, Co-operative Group, Fujitsu, Marconi, Mitsubishi Electric and IPWireless - a broad range of services from high-end applications to innovative product development and technical consultancy skills. For ten years, its multi disciplinary team of hardware and software engineers have provided cost-effective solutions from concept through to pre-production.

What is JTAG?

Advances in silicon design, such as increasing device density and, more recently, ball grid array (BGA) and chip scale packaging, have reduced the efficacy of traditional electronic circuit testing methods. In order to overcome these problems and others; some of the world's leading silicon manufacturers combined to form the Joint Test Action Group (JTAG). The findings of this group were used as the basis for the Institute of Electrical and Electronic Engineers (IEEE) standard 1149.1: Standard Test Access Port and Boundary Scan Architecture and subsequently the standard became known as JTAG.

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